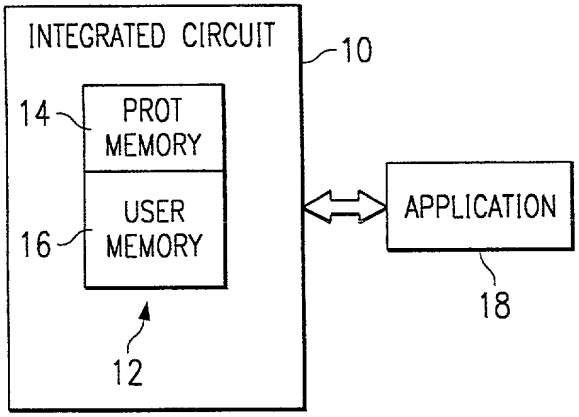


FIG. 1

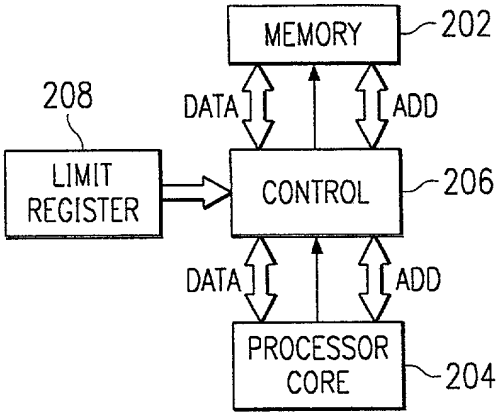


FIG. 2

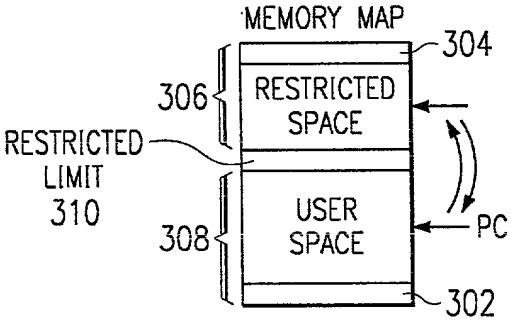


FIG. 3

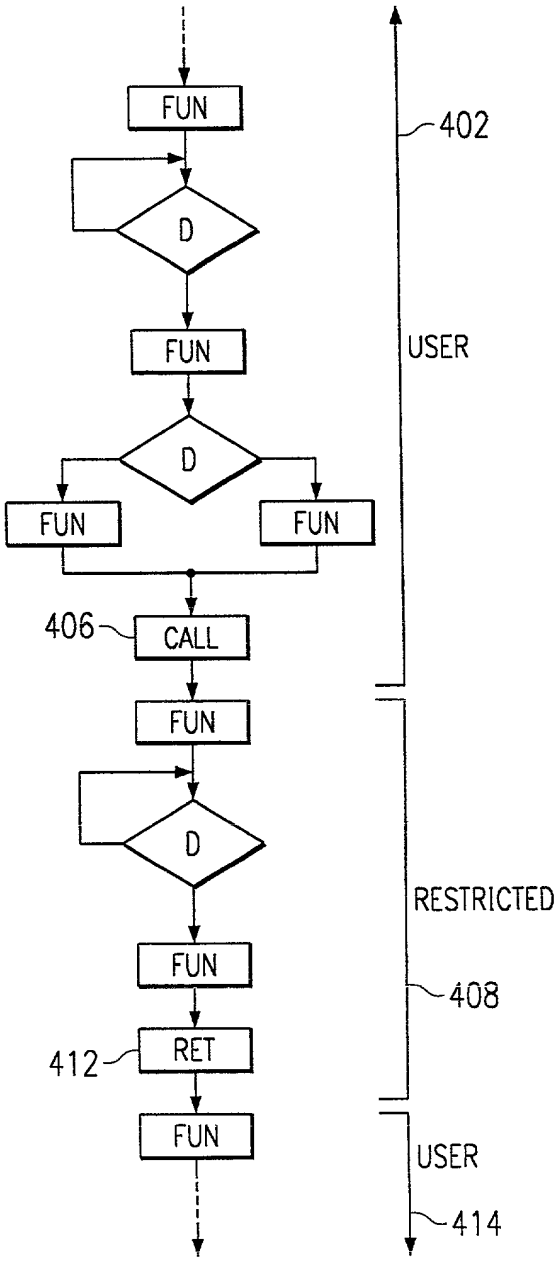
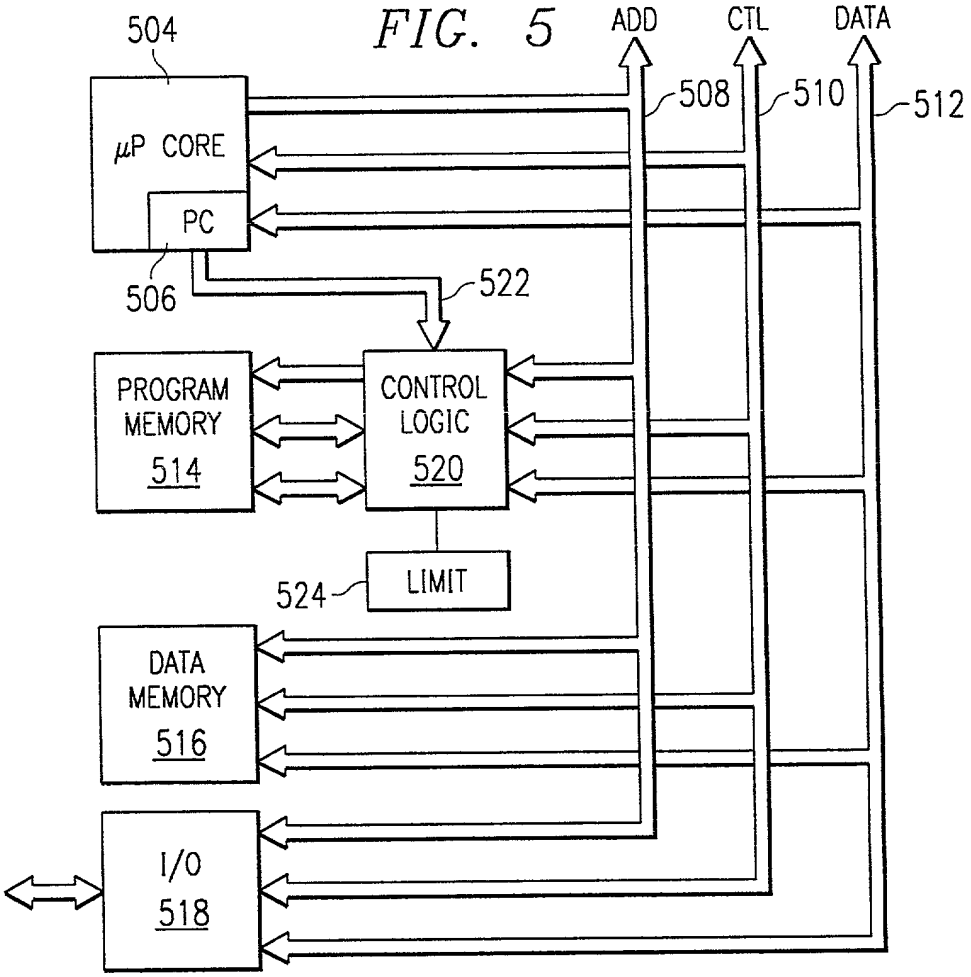


FIG. 4

Express Mail Label No. EL 996 760 760

FIG. 5



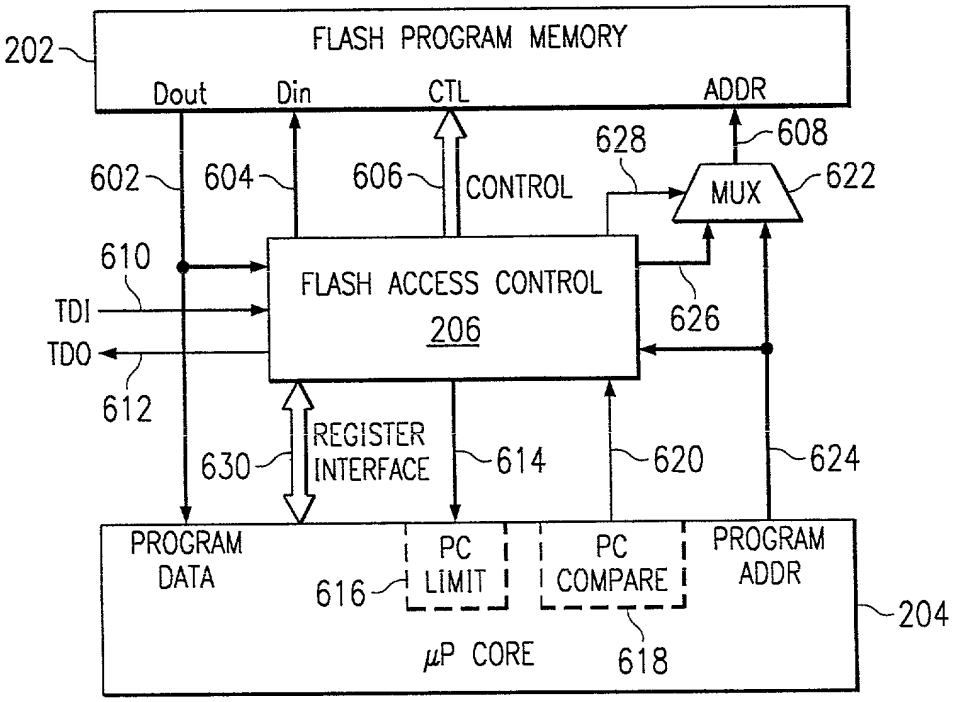


FIG. 6

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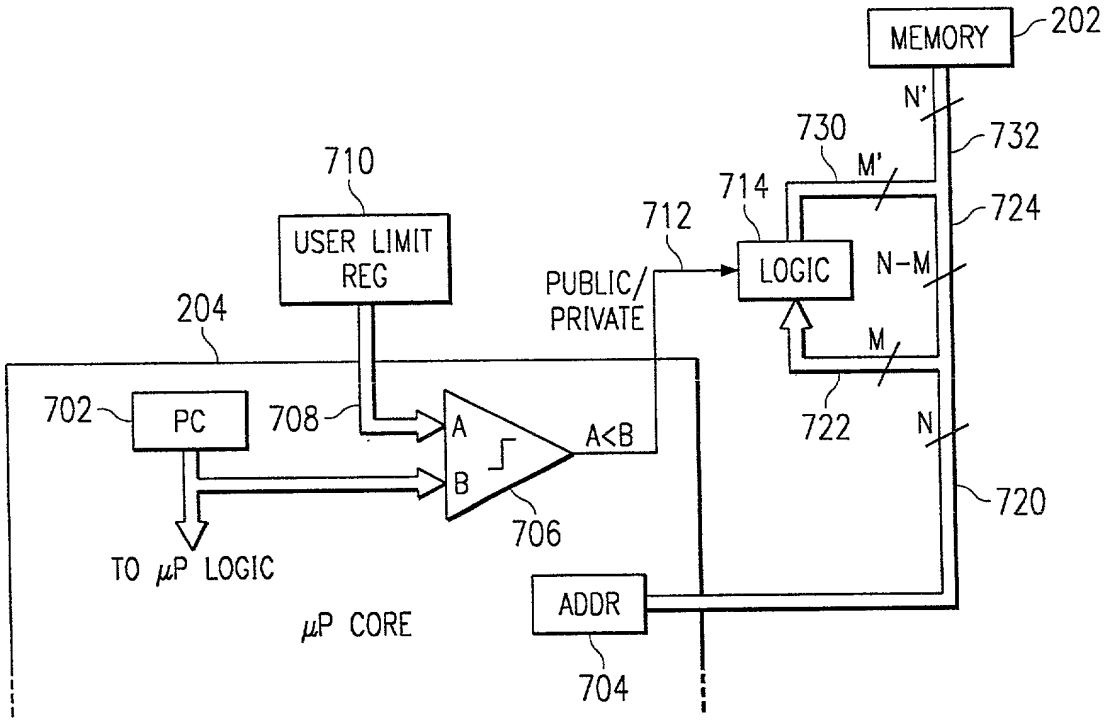
MEMORY
202
N'
730
M'
732
710
USER LIMIT REG
714
724
712
LOGIC
N-M
PUBLIC/ PRIVATE
204
M
702
PC
708
A
A<B
722
N
B
706
720
TO μP LOGIC
μP CORE
ADDR
704

FIG. 7

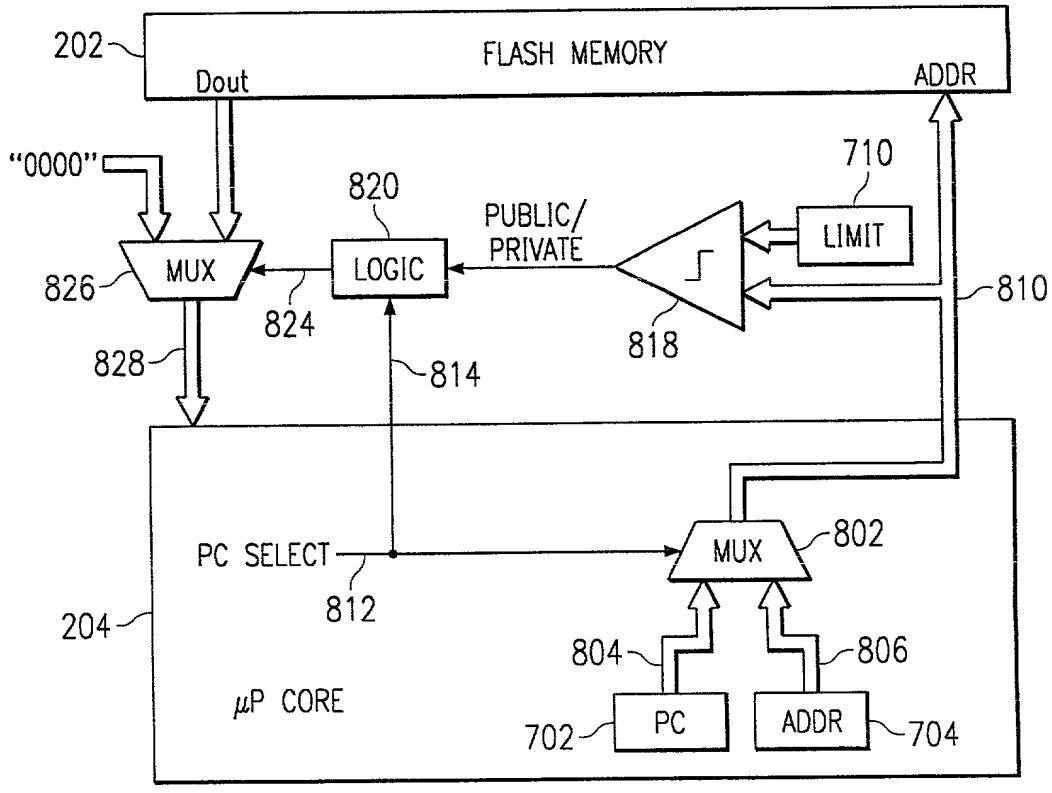
202
FLASH MEMORY
Dout
ADDR
"0000"
710
820
PUBLIC/ PRIVATE
LIMIT
MUX
826
LOGIC
824
818
810
828
814
PC SELECT
MUX
802
812
204
804
806
μP CORE
702
PC
ADDR
704

FIG. 8

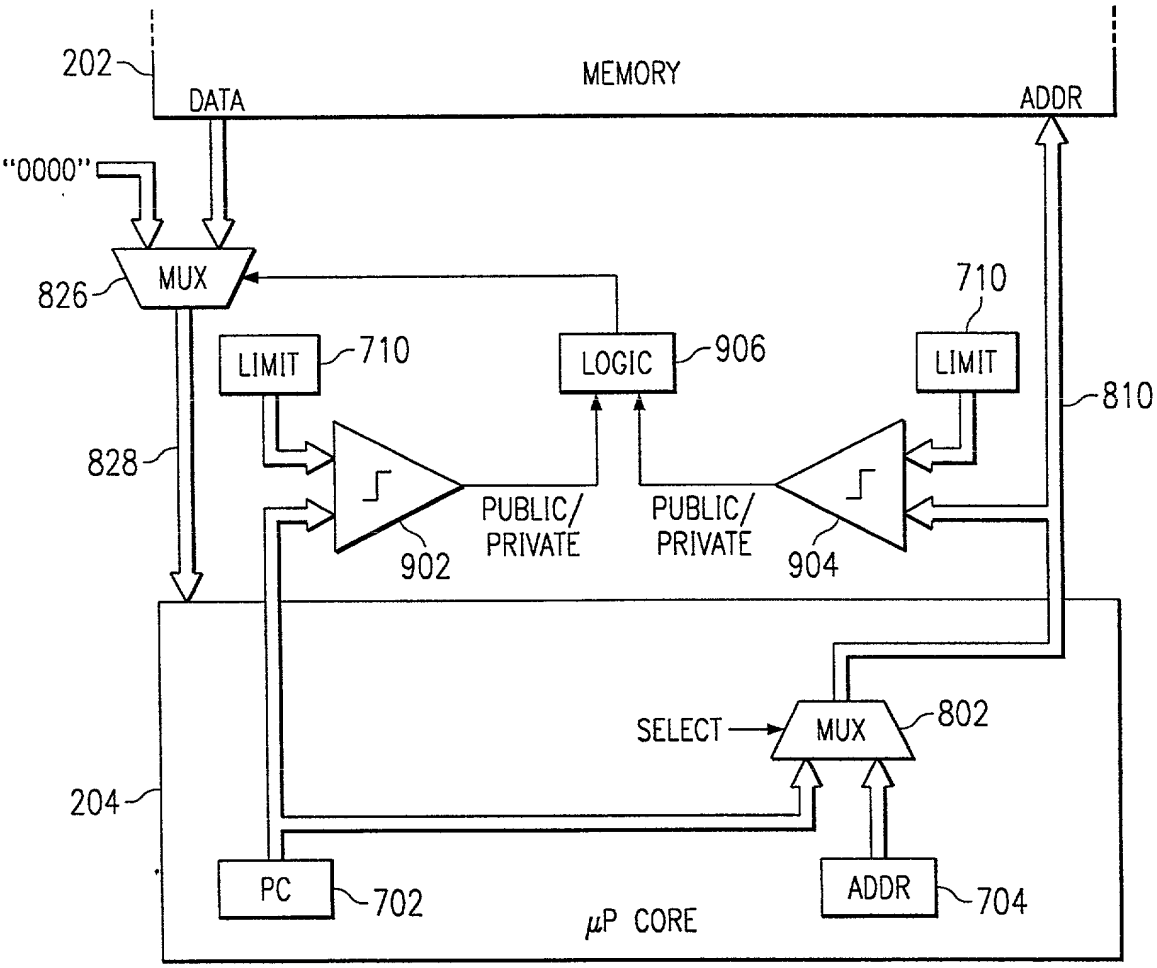
202
MEMORY
DATA
ADDR
"0000"
826
MUX
710
LIMIT
710
LIMIT
LOGIC
906
810
828
PUBLIC/
PRIVATE
PUBLIC/
PRIVATE
902
904
SELECT
MUX
802
204
PC
702
ADDR
704
μP CORE

FIG. 9

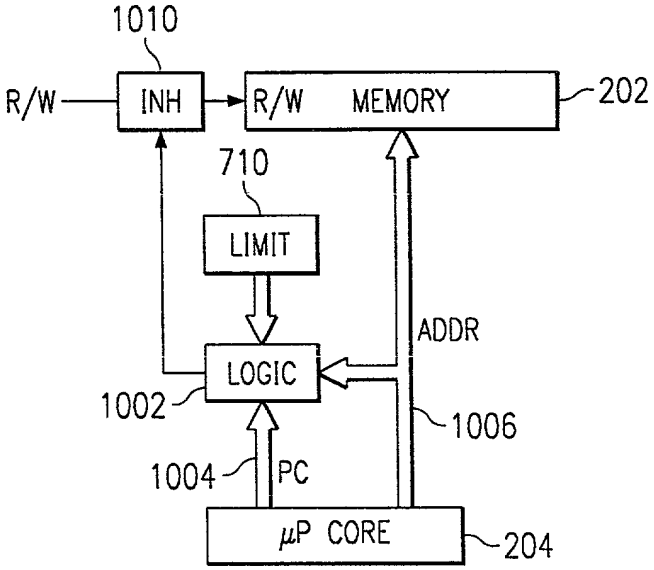
1010
R/W
INH
R/W MEMORY
202
710
LIMIT
ADDR
LOGIC
1002
1006
1004
PC
μP CORE
204

FIG. 10

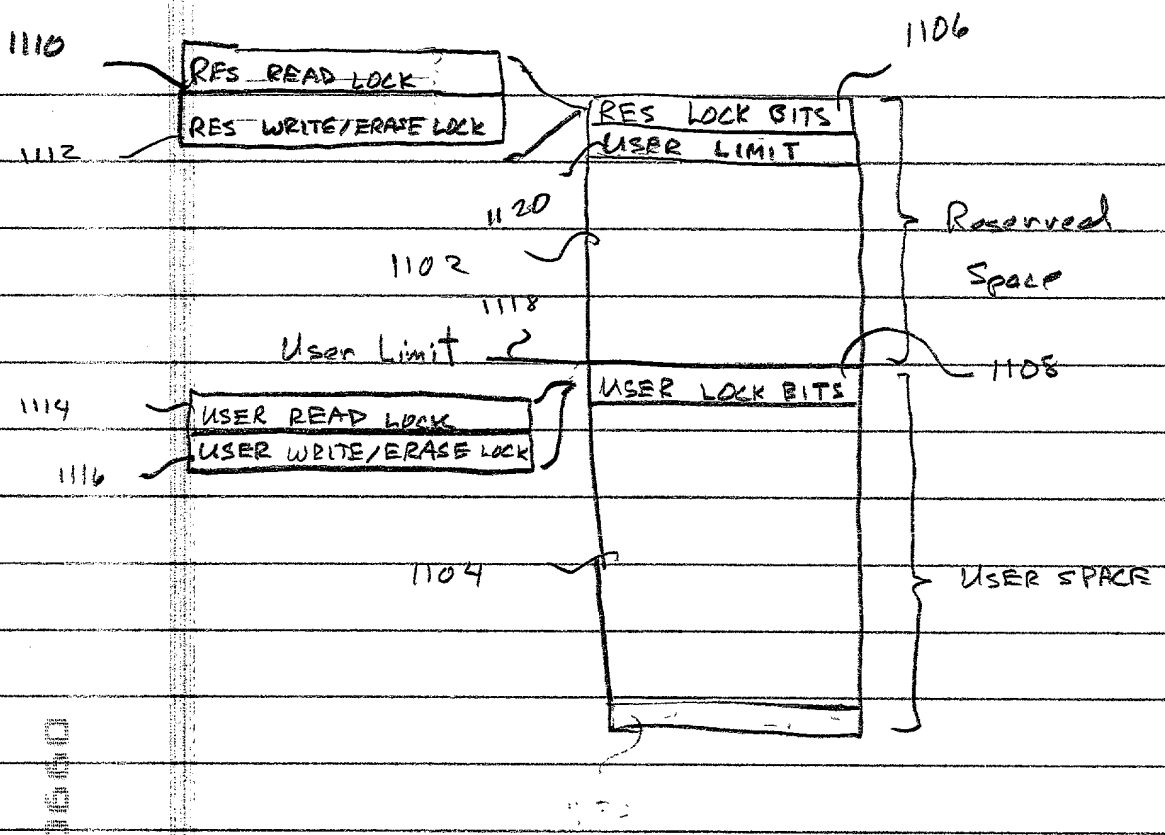
1110
RES READ LOCK
RES WRITE/ERASE LOCK
1112
1106
RES LOCK BITS
USER LIMIT
1120
1102
1118
User Limit
Reserved
Space
1108
USER LOCK BITS
1114
USER READ LOCK
USER WRITE/ERASE LOCK
1116
1104
USER SPACE

FIG 11

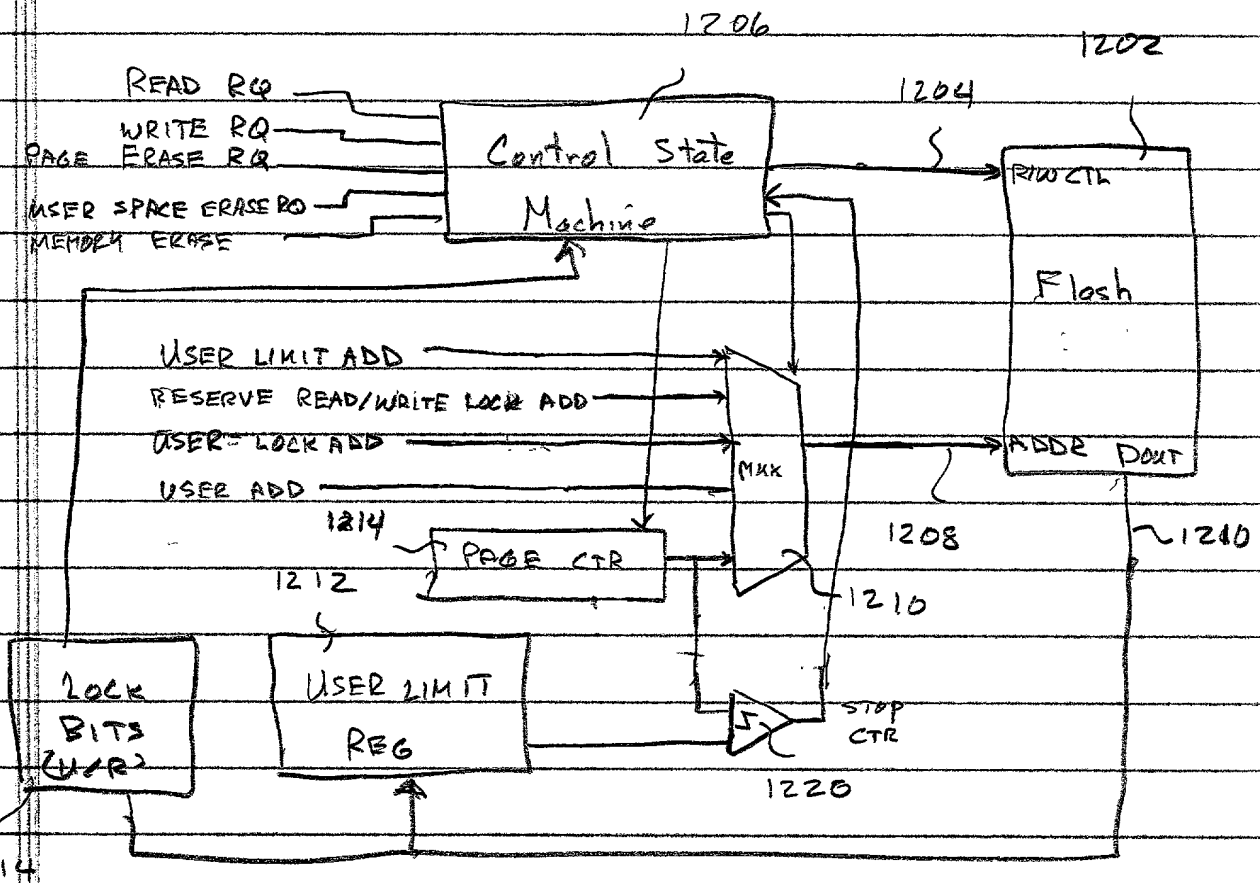
1206
1202
READ RQ
WRITE RQ
PAGE ERASE RQ
USER SPACE ERASE RQ
MEMORY ERASE
Control State Machine
1204
R/W CTL
Flash
USER LIMIT ADD
RESERVE READ/WRITE LOCK ADD
USER LOCK ADD
USER ADD
MUX
ADDR DOUT
1214
PAGE CTR
1208
1210
1212
1210
LOCK BITS (W/R)
USER LIMIT REG
STOP CTR
1220
1214

FIG 12

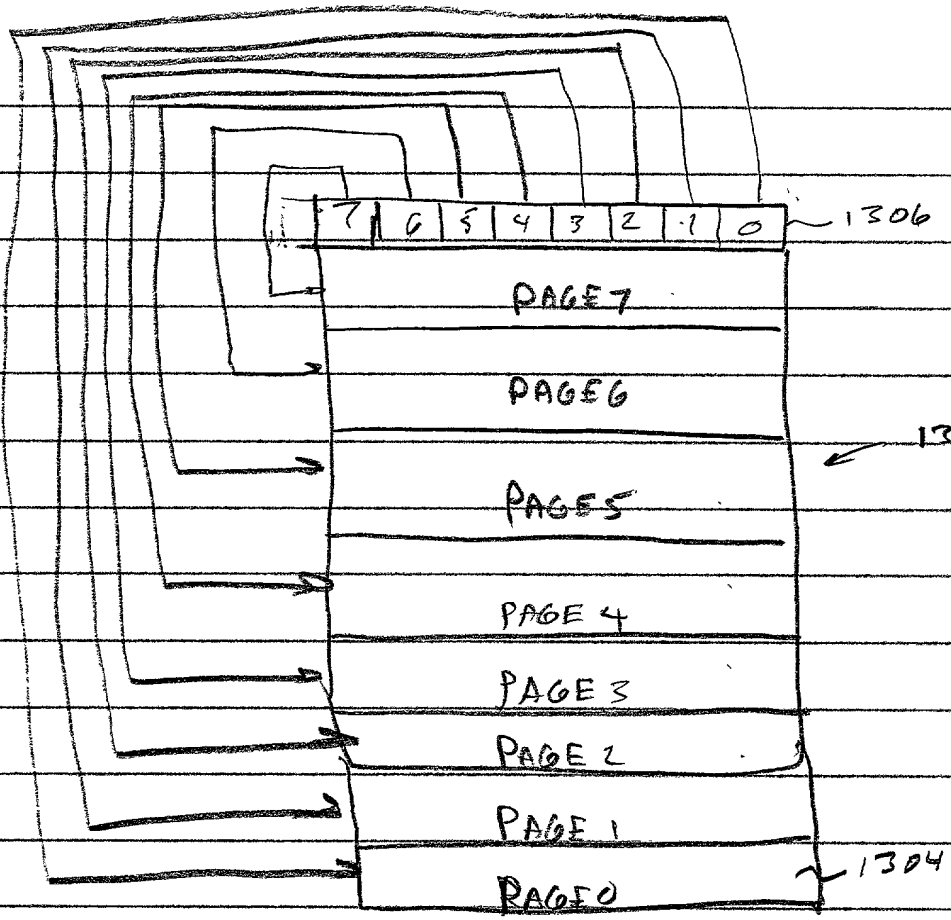

FIG 13

Patent Application Publication

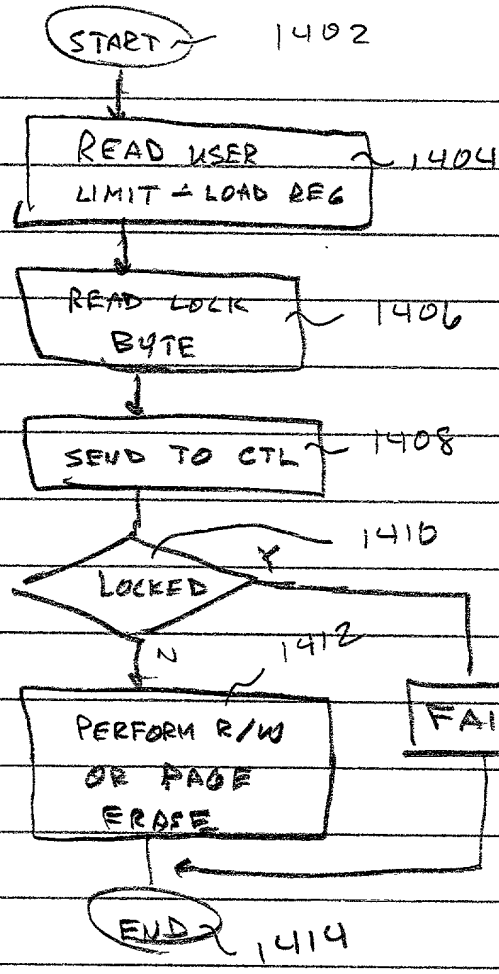
START
1402
READ USER LIMIT → LOAD REG
1404
READ LOCK BYTE
1406
SEND TO CTL
1408
LOCKED
1410
Y
N
1412
PERFORM R/W OR PAGE ERASE
FAIL
1411
END
1414

FIG 14

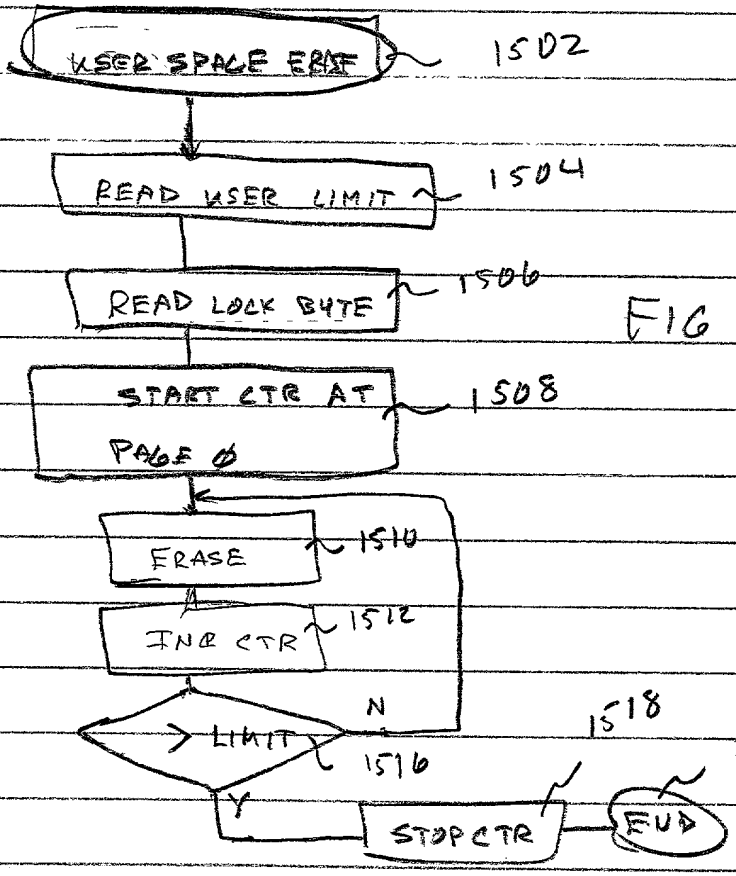
USER SPACE ERASE
1502
READ USER LIMIT
1504
READ LOCK BYTE
1506
START CTR AT PAGE 0
1508
ERASE
1510
INR CTR
1512
> LIMIT
N
Y
1516
1518
STOP CTR
1520
END

FIG 15